REMARKS

Claims 26-44 are currently pending in this application. In the last Office Action, claims 42-44 were objected to due to informalities. In addition, claims 26-27, 31, 34-35, 38, and 42-43 were rejected under 35 U.S.C. 102 as anticipated by U.S. Pat. No. 5,895,487 (Boyd). The Examiner indicated that claims 28-30, 32-33, 36-37, 39-41, and 44 would be allowable if rewritten in independent form including all of the limitations of the base claims. Applicant thanks the Examiner for this indication of allowability.

While Applicant does not necessarily agree with the rejections in the last office action, this Response amends claims 26, 28, 29, 31, 33, 34-37, and 42 to focus on different aspects of the Applicant's invention, correct typographical errors, and to expedite prosecution of this application. Applicant submits that these amendments address the informalities objections raised in the last Office Action.

1. Reasons why the rejection of claims 26-30 and 42-44 should be withdrawn

Claims 26-30 and 42-44 were rejected as anticipated by Boyd. In this regard, the last office action relied upon the multiprocessor system shown in FIG. 5 of Boyd and upon the accompanying description in col. 6 of the Boyd specification. Applicant submits that these rejections should be withdrawn for at least the following reasons.

Applicant submits that the "global tag array 52" disclosed in Boyd does not constitute the "merged tag array" recited in amended claims 26 and 42 of the present application. Among other things, claims 26 and 42 recite a merged tag array that is to store "a plurality of entries that each contain directory information for the first data array and the second data array" (emphasis added). By contrast, the global tag array 52 in Boyd "has entries for each of the individual L2 caches." *See* Col. 6, ln. 17-19. Thus, Boyd's while global tag array 52 contains a plurality of tags 1 to N, each tag corresponds to a different L2 cache. In other words, "tag 1" in global tag array 52 corresponds to "tag 1" in processor 51_1, "tag 2" in global tag array 52 corresponds to "tag 2" in processor 51_2, etc. The tags in global tag array 52 do not each contain directory information for both a first data array and a second data array as recited in

claims 26 and 42 of the present application. Thus, Boyd does not disclose these limitations of claims 26 and 42.

For at least these reasons, claims 26 and 42 are believed to be patentable. Claims 27-30 and 43-44 depend from one of claims 26 and 42 and are patentable for at least the same reasons as claims 26 and 42, as well as for additional limitations contained therein.

2. Reasons why the rejection of claims 31-33 should be withdrawn

Claims 31-33 were rejected as anticipated by Boyd. Applicant submits that these rejections should be withdrawn for at least the following reasons.

As discussed above, Applicant submits that the "global tag array 52" disclosed in Boyd does not constitute the "merged tag array" recited in claim 31. Among other things, amended claim 31 recites a merged tag array that is to store a plurality of entries, with "each of said entries" comprising "a first directory field containing information about the contents of a corresponding set in a first data array" and "a second directory field containing information about the contents of a corresponding set in a second data array" (emphasis added). The global tag array 52 in Boyd contains a plurality of tags 1 to N, but these tags do not each contain directory information about the "contents of a corresponding set in a first data array" and "the contents of a corresponding set in a second data array" as recited in claim 31. Thus, Boyd does not disclose these limitations of claim 31.

For at least these reasons, claim 31 is believed to be patentable. Claims 32-33 depend from claim 31 and are patentable for at least the same reasons as claims 31, as well as for additional limitations contained therein.

3. Reasons why the rejection of claims 34-37 should be withdrawn

Claims 34-37 were rejected as anticipated by Boyd. Applicant submits that these rejections should be withdrawn for at least the following reasons.

Claim 34 recites a system comprising a "first level cache array", a "second level cache array" and "a third array to store tags for both the first level cache array and the second level cache array" (emphasis added). By contrast, Boyd's global tag array 52 does not store tags for a first level cache array and a second level cache array as recited in claim 34. Rather, Boyd discloses a "global tag array 52 that has entries for each of the individual L2 caches" (emphasis added). Boyd's global tag array 52 does not contain any information for any of the L1 caches shown in Boyd's FIG. 5. Thus, Boyd does not disclose these limitations of claim 34.

For at least these reasons, claim 34 is believed to be patentable. Claims 35-37 depend from claim 34 and are patentable for at least the same reasons as claims 34, as well as for additional limitations contained therein.

4. Reasons why the rejection of claims 38-41 should be withdrawn

Claims 38-41 were rejected as anticipated by Boyd. Applicant submits that these rejections should be withdrawn for at least the following reasons.

Claim 38 recites a method comprising "issuing a request for information to a first data array, a second data array, and a merged tag array" and then "determining from the merged tag array whether the request generated a cache hit in the first data array or second data array" (emphasis added).

Boyd does not issue a request for information to two data arrays and then determine whether the request generated a cache hit in the first data array or second data array. Rather, Boyd describes the sequence of operations for the MP configuration of FIG. 5 as follows:

"For processor i hit, the data will be found in the L1 SRAM cache.

For a miss in L1 cache, got (sic) to the L2 tag array for the processor.

If there is a hit in the L2 tag array, continue.

If there is a miss in the L2 tag array, go to the global tag array.

If there is a hit in the global tag array, the data resides in the L2 cache of another processor and must be retrieved.

If there is a miss in the global tag array, data must be retrieved from main memory or a lower level in the memory hierarchy." Col. 6, lns. 31-44 (emphasis added).

In other words, in Boyd a request for information from the L2 cache for proc 1 (for example) is made only if there is a miss in the L1 cache for proc 1, and a request for information is made to the L2 cache of another processor only if the L2 cache of proc 1 does not have the data. Boyd does not make a request for information to two data arrays and then determine whether the request generated a cache hit in the first data array or second data array as recited in claim 38. Thus, Boyd does not disclose these limitations of claim 38.

For at least these reasons, claim 38 is believed to be patentable. Claims 39-41 depend from claim 38 and are patentable for at least the same reasons as claims 38, as well as for additional limitations contained therein.

5. Conclusion

Applicant respectfully requests entry of the above amendments and favorable action in connection with this application. The Examiner is invited to contact the undersigned at (202) 220-4310 to discuss any matter concerning this application. The

Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. § 1.16 or § 1.17 to Deposit Account No. 11-0600.

Respectfully submitted,

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